

Improving Prediction of Semiconductor Lifetimes

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We want our electronic gadgets to function properly for long periods of time, and service lifetimes are particularly critical where systems must work reliably far longer. It is thus important to know how long integrated circuits (ICs) will function properly. It's not practical to test ICs in the reality conditions and thus wait years to find out when failures start to occur naturally or through operation. Semiconductor engineers have consequently developed accelerated life-cycle tests, which place components under high current stress and temperature. This helps predict their useful lifetimes by extrapolation. Based on such experiments we have also started to develop models that predict semiconductor lifetimes.

These models don't predict when a specific device will fail, but can predict, with reasonable certainty, the rate of failure under specific conditions. And semiconductor companies are expending a great deal of effort to make these models as accurate as possible. In order to do so, process engineers need a better understanding of the underlying failure mechanisms. With the help of COMSOL Multiphysics, myself and others at the \$10 billion company STMicroelectronics are studying the mechanisms that bring about one of the primary causes for IC failure, electromigration in interconnects.

A complex multiphysics problem

With the scaling down of semiconductor devices, current density in the metal interconnects joining individual transistors increases. Up to now, lifetime models have been based on empirical methods. Thus, an evaluation of potential failure modes is very important as STMicroelectronics brings new advanced CMOS technologies onto the market.

In devices fabricated with these process technologies, interconnect copper lines can be just 100nm thick and roughly the same height. The prevalent failure mode for interconnects is electromigration, which is the net transport of material caused by conducting electrons colliding

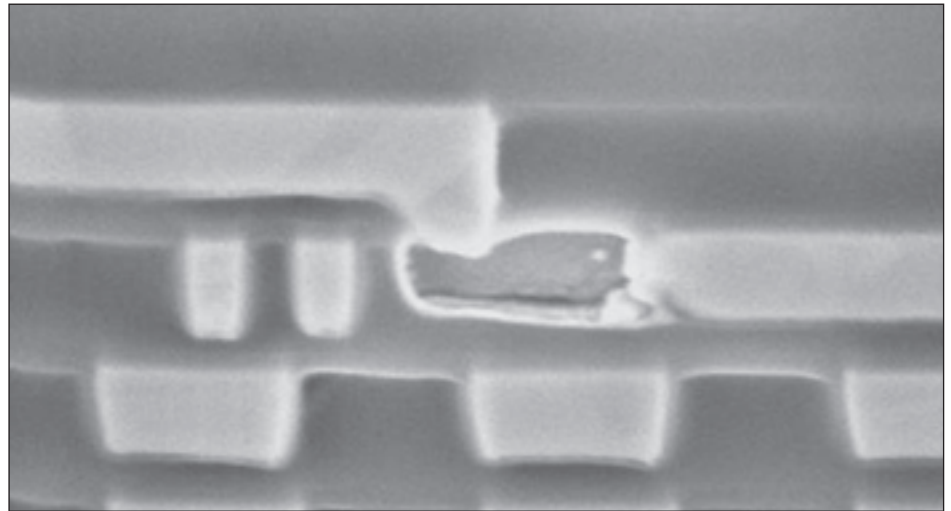


Figure 1: A scanning electron microscopy image of a copper line interconnect where a void has developed due to vacancy accumulation. This has led to a broken circuit.

with metal ions. Over time, a number of metal atoms are knocked from their original positions due to this phenomenon commonly known as an “electron wind.” The subsequent vacancies or holes in the crystal structure are due to the migration of metal atoms, and over time, these can accumulate to form minute voids that lead to open circuits and device failure, see Figure 1. Vacancy flux depends on several driving forces including the gradients of the hydrostatic stress, temperature and electric potential.

Several characteristics of the metal interconnect have a strong influence on their lifespan. These include the conductor's dimensions, the material properties, the electrochemical deposition process, and the chemical mechanical planarization (CMP) process used to fabricate the interconnects.

When our reliability engineers per-

form accelerated life tests, they want to work with worst-case conditions. With the deeper understanding of electromigration we gain with our multiphysics model, we can be much more certain that we have actually stipulated the worst-case conditions.

Realistic simulation of the microstructure

We chose COMSOL Multiphysics because it was able to efficiently handle all

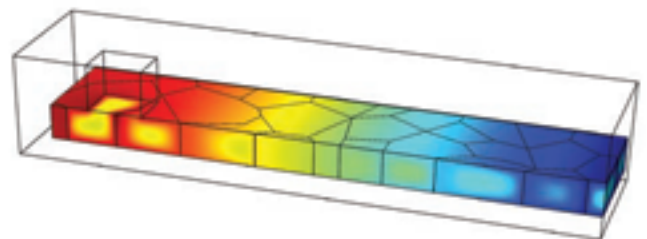


Figure 2: The extent of relative vacancy concentration through a copper interconnect line connected to the via and embedded in oxide. The higher relative vacancy occurs in the vicinity of the via, which is to be expected. Yet, areas of relative vacancy concentration are also prevalent at the boundaries between grains.

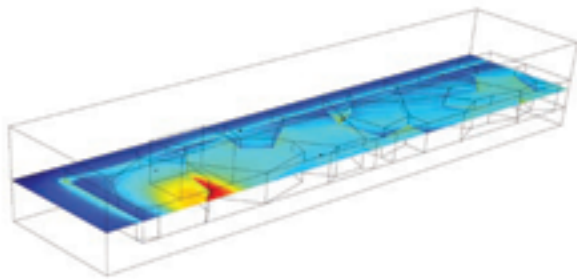


Figure 3: von Mises stresses in a slice through the copper interconnect line. Areas of greatest stress occur close to the via at the first grain boundary.

the physical factors that influence electron migration in metallic interconnects. Our model couples the transport of vacancies with structural mechanics and thermal diffusion. We started with a 2D model that enabled us to benchmark the solution and gain confidence in the approach. However, realistic diffusion paths involve multiple metal/metal interfaces, which drove us to create a 3D model, where we studied the transient vacancy transport with realistic microstructure and kinetic paths, see Figure 2.

The model couples several physics: standard diffusion due to concentration gradients; the “electron wind” driven by a chemical potential difference; hydrostatic stress and heat-induced atomic diffusion. COMSOL Multiphysics provides a number of tools for modeling such phenomena: the ease of creating a geometry that accounts for crystal grains and interfaces between different components, such as interconnects and vias; the ease of modeling different coefficients (for both electromigration and structural mechanics); and the ease of modeling multiphysics phenomenon (coupling the diffusion equations from the DC current to the physics of structural mechanics and heat transfer), see Figure 3.

After studying the model results, we learned that, as a first approximation, the location of the void nucleation can be determined by the occurrence of a critical vacancy concentration. The model enables us to predict that maximum concentration as a function of applied current, initial stress, temperature and, above all, the line’s geometry. As a result, we now have a preliminary predictive model for

the lifetime of metal interconnects, see Figure 4.

These modeling results are important to our reliability teams because our accelerated tests must be very predictive and accurate. However, there are many physical effects engineers don’t yet fully understand. We are currently using COMSOL Multiphysics to develop better predictive failure models so that we can save time in our qualification process and also be sure that we are indeed using worst-case scenarios. With the help of these models we also get insight into process design rules that define, for instance, the minimum size for interconnects.

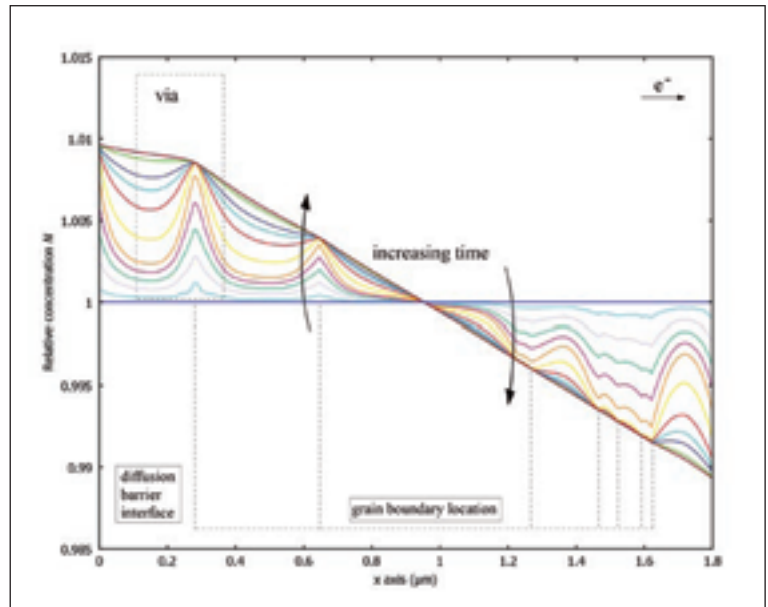


Figure 4: The evolution of relative vacancy concentration along a line through the center of the model. The peaks occur close to the via and in the vicinity of the grain boundaries.

The modeling team

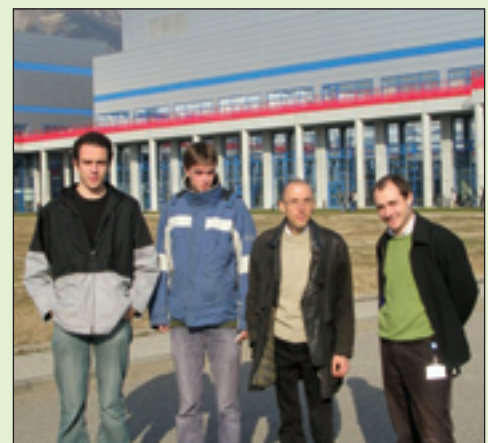
Hired by STMicroelectronics specifically to do mechanical and thermal simulation, the two authors are part of the modeling team at the company’s site in Crolles, France. They spend roughly 60% of their time simulating semiconductor aspects such as thermal effects and Joule heating, as well as nonlinear mechanical effects. ■

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About the Authors

Florian Cacho received his Ph.D. in Material Science from l’Ecole des Mines de Paris. Since 2005, he has been a mechanical & thermal engineer in the Technology Modeling Department at STMicroelectronics in Crolles, France.

Vincent Fiori has a masters degree in Mechanical Engineering from the National Institute of Applied Science, Lyon. He joined STMicroelectronics in 2000 and currently leads projects on mechanical and thermal modeling activities. These are particularly focused on the front-end technology development of semiconductor production.



The modeling team at STMicroelectronics standing outside their facility in Crolles, France. From left: Sébastien Gallois, Romuald Roucou, Vincent Fiori and Florian Cacho.